REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed December 28, 2005.

Drawings

The drawings are objected to for failing to include a feature described in the claims. Claim 18 is amended to exclude the feature "audio device". Therefore, Applicant submits the objection is overcome.

Claim Objections

Claims 18-25 are objected to because of the inclusion of the limitation "audio device" in claim 18. The term "audio device" has been removed from the claims. Therefore, Applicant submits that the rejection is overcome.

35 U.S.C. 102 Rejections

Claims 1-31 are rejected under 35 U.S.C. §102(b) as being anticipated by Nakamura (U.S. patent No. 5,627,841). Specifically, the Office Action asserts that Nakamura anticipates all elements of claims 1, 8, 18, 26, including those elements related to the functional clock and scan signals being controlled independently of each other.

Claim 1 is presently amended to reflect that the first and second control means enable one functional unit to be tested while other functional units that use the same functional clock may operate normally. Nakamura, on the other hand clearly shows in Figure 3 and throughout that the one user clock (functional clock) is used to clock combinational logic flip-flop (functional

unit) 1, which is tested by scan logic 22 and 23, while another user clock is used to operatate the untested logic 5 and 6 (other functional units). Indeed, it is not the goal of Nakamura, nor is it taught in Nakamura, for the functional units to be clocked by the same clock while one or more of the functional units are tested using a scan chain. In fact, Nakamura relies on there being more than one functional clock to test the various functional units. Therefore, claim 1 as amended, and for similar reasons, claim 18, are not anticipated by Nakamura.

As for claim 8, Nakamura makes no mention of a scan clock hierarchy that enables independent testing of functional units. In fact, Nakamura only teaches a series of flip-flops corresponding to some combinational logic that may be tested using scan flip-flops. Furthermore, Nakamura makes no mention of the scan clocks being operated at different speeds. Because the flip-flops illustrated in Nakamura are in series, it would appear impossible for the scan clocks to operate at different speeds, else the data passed between the serial flip-flops would not be latched properly. Regardless, Nakamura does not teach that the scan clocks are operated at different speeds as claimed in claim 8. Accordingly, Applicant submits that Nakamura does not anticipate claim 8.

As for claim 26, Nakamura does not teach a plurality of scan clock speeds, as previously mentioned in regard to claim 8, nor does Nakamura teach any of the ITC, CTC, UTC, LTCC logic as claimed in claim 26. Nakamura teaches a small series of flip-flops, the functional clocks of which, are gated by the SCD 11, 13 units. However, nowhere in Nakamura are any other control logic mentioned, much less those explicitly mentioned in claim 26. Accordingly, Applicant submits that Nakamura does not anticipate claim 26.

Because Nakamura fails to teach that which is claimed in claim 1, as presently amended, nor that which is claimed in claims 8, 18, and 26, Applicant respectfully submits the rejection is overcome.

Accordingly, it is respectfully asserted by Applicant that claims 1-31 are in condition for allowance.

If there are additional fees due, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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